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<b>title</b> LOGARITHMIC ROUTINE FOR THE 2650 MICROPROCESSOR					
<b>author</b> E.D. van Veldhuizen					
<b>summary</b> This report describes a possible routine for calculating the $e^{\log (\ln)}$ of BCD floating point numbers by means of the CORDIC algorithm. The format of the floating point numbers (input number as well as result) is the same as used in the arithmetic routines described in EDP 7603 by A.F. Craens. These arithmetic routines are used in the log routine and must be present in the program store to execute the log function.					
E.D. van Veldhuizen					
Advies Octrooi d.d. <b>31 jan. 1977</b>	X AV	GV	B	BL	
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Datum: <b>11 jan. 1977</b>	Mamo				

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CONTENTS:

	<u>PAGE</u>
1. Introduction	R 2
2. References	R 2
3. Interfaces	R 2
3.1. Format	R 2
3.2. Input/Output variables	R 3
3.3. PSW and registers	R 3
3.4. Error signalling	R 4
4. Function	R 4
5. Performance	R 6
5.1. Accuracy	R 6
5.2. Timing	R 6
6. Remarks	R 6
7. Flowchart	R 7 ,8
8. Program	R 9

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## 1. INTRODUCTION

The log of a BCD floating point number is calculated using the CORDIC algorithm as described in references nr. 2 and nr. 3.

The interfaces to the program which uses the log routine are such, that calling the routine gives as little overhead as possible in time as well as in program store.

Also the status of the calling program is saved.

In describing the function, the algorithm is given in BASIC. Boundaries and scaling of input numbers are indicated. Accuracy and timing are given to indicate the performance of the routine.

Finally the actual program is described in flowcharts and given in assembly language.

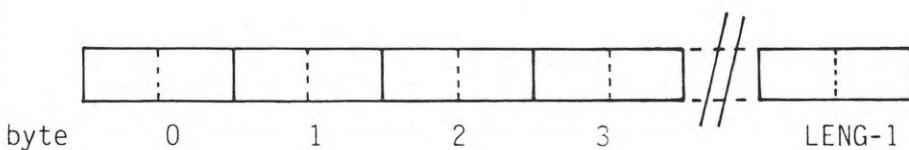
## 2. REFERENCES

- 2.1. BCD Floating point arithmetic for the 2650 microprocessor by A.F. Craens. EDP 7603.
- 2.2. The CORDIC trigonometric computing Technique by J.E. Volders IRE transactions on electronic computers, September 1959.
- 2.3. Use decimal CORDIC for generation of many transconductance functions by H. Schmidt and A. Bogacki. EDN, February 20, 1973.

## 3. INTERFACES

### 3.1. Format

The format of the BCD floating point numbers as given in reference nr. 1, is as follows:



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Byte 0: sign of exponent ( $=H'000$ ,  $=H'F0'$ )  
1: exponent (absolute, 2 digits)  
2: sign of mantissa ( $H'00'$  or  $H'F0'$ )  
3: two most significant digits of mantissa  
LENG-1: two least significant digits of mantissa

The length of the floating point number can be set by defining the LENG constant in the BCD arithmetic floating point package. The length of the mantissa will be  $(LENG-3) * 2$  digits. The exponent always has two digits. The input number should always be left-normalized.

### 3.2. Input/Output variables

When calling the log routine, R0 and R1 of the selected bank should contain the address of byte 0 of the input number. R0 holds the most significant part and R1 the least significant part of the address. R2 and R3 should contain the address of byte 0 of the result location. R2 holds the most significant part and R3 the least significant part of the address. Register select is don't care.

### 3.3. PSW and registers

When entering the log routine the current PSL is saved and before returning, it will be restored including the condition code. PSU is not affected.

The registers belonging to the selected bank and R0 are changed and are not restored.

The registers of the bank which was not selected are not affected.

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### 3.4. Error signalling

When an error occurs, because a negative or zero number appears as an operand, a jump is made to location ERR.

However, no return from subroutine has been made before the jump to ERR.

The location ERR has to be defined in the main program.

### 4: FUNCTION

When the log routine is entered, input and output addresses as present in R0, R1, R2 and R3 are stored and the Program Status Register is saved.

Then the input number is scaled up or down to bring it in the region between +0.1 and +1. For each multiplication by 10 (increment of exponent by 1),  $\ln 10$  is subtracted from the result output.

For each division by 10 (decrement of exponent by 1),  $\ln 10$  is added to the result output.

Also the number is screened whether it is negative, zero or one. If negative or zero, the routine jumps to location "ERR", which should be defined by the main program, and no return from subroutine is made.

If the number is 1 (after scaling in fact. 0.1),  $\ln 10$  is subtracted from the result output and a return is made.

For the purpose of the algorithm as given below, a table T of 8 constants has been loaded and forms a part of the program. For each item of the table applies:

$T(I) = \tanh(T)$  where T initially is 0.1 and for the next I  
 $T = T/10$ .

The actual log calculation is done by means of the following algorithm.

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Input number is A.

7000

X = A-1

Y = A+1

U = 0

Z = 0.1

J<sub>9</sub> = 22

N = 8

For I = 1 to N

For J = 1 to J<sub>9</sub>

If Y > 0 then go to P

If X < 0 then go to Q

S U = U - T(I)

X<sub>1</sub> = X + Y \* Z

Y<sub>1</sub> = Y + X \* Z

Go to R

P If X < 0 go to S

Q U = U + T(I)

X<sub>1</sub> = X - Y \* Z

Y<sub>1</sub> = Y - X \* Z

R X = X<sub>1</sub>

Y = Y<sub>1</sub>

Next J

Z = Z/10

J<sub>9</sub> = 9

Next I

Output = U+U

End

This algorithm follows from the description given in reference 3. It is implemented in assembly language as indicated in the flowcharts.

First the operand is brought in the range of 0.1 → 1.0. Each time the exponent is increased by 1, ln 10 is subtracted from the output result.

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If the exponent is decreased,  $\ln 10$  is added to the output result. Addition or subtraction of U and T(I) is determined by the signs of X and Y being equal or not.

## 5. PERFORMANCE

### 5.1. Accuracy

The accuracy of the calculated result has been investigated by taking 100 log calculations ( $\log+00+01000000$  ----  $\log+01+10000000$ ).

On average the error is less than 1 in  $3 \cdot 10^6$ .

Worst case the error could be 1 in  $4 \cdot 10^3$ .

### 5.2. Timing

The execution time of the log routine ranges from 4 ms ( $\log+01+10000000$ ) to about 6 seconds ( $\log+90+99999999$ ).

The average execution time is about 2 - 2.5 seconds.

Accuracy and timing have been measured with 8-digit mantissa. With less digits the accuracy will deteriorate but the timing will improve.

## 6. REMARKS

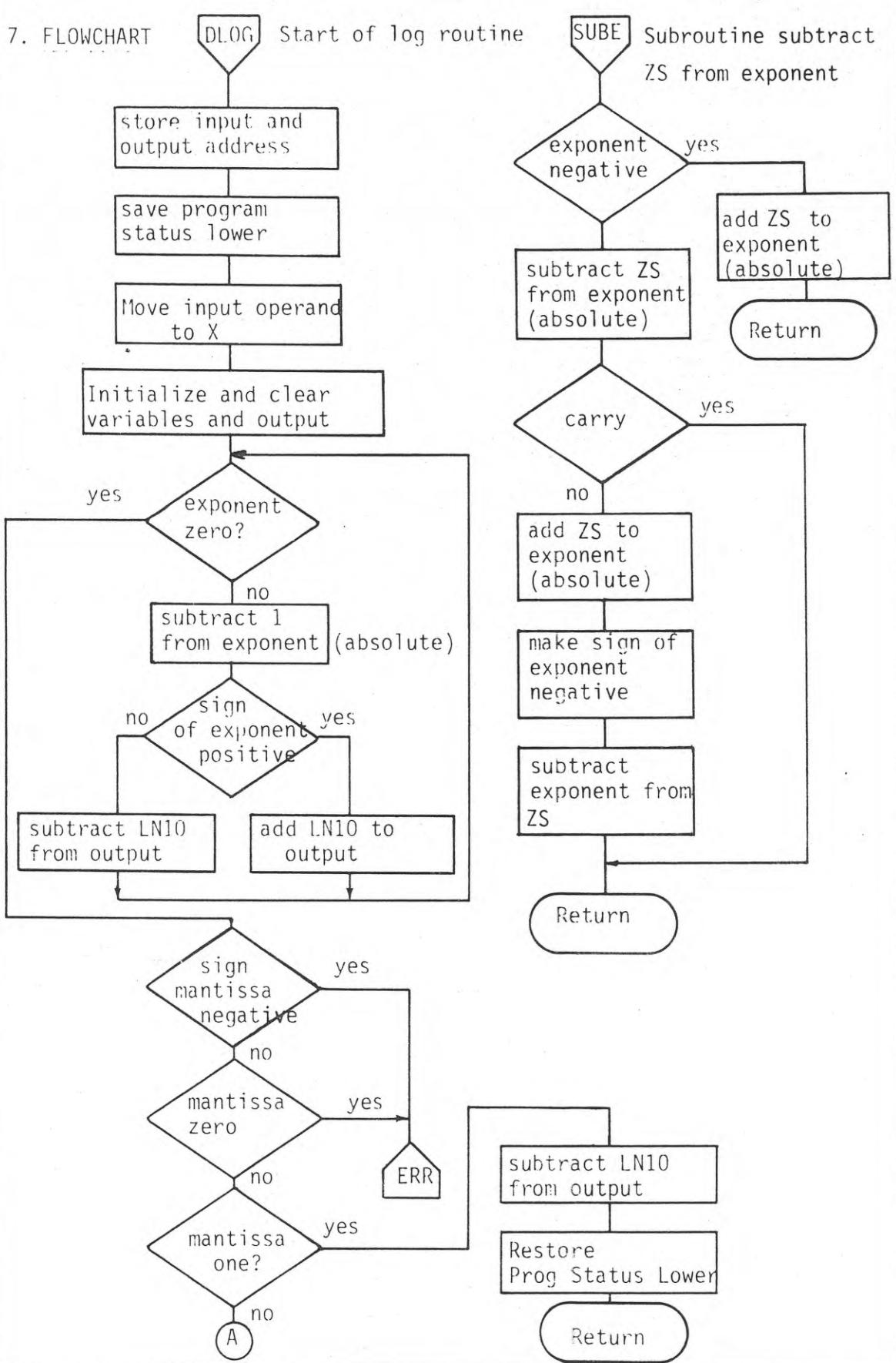
The CORDIC algorithm and existing floating point routines were used on request from Signetics. The present routine was made as an exercise to get some indication about execution time and accuracy. As is shown in section 5, this approach does not seem to be very suitable.

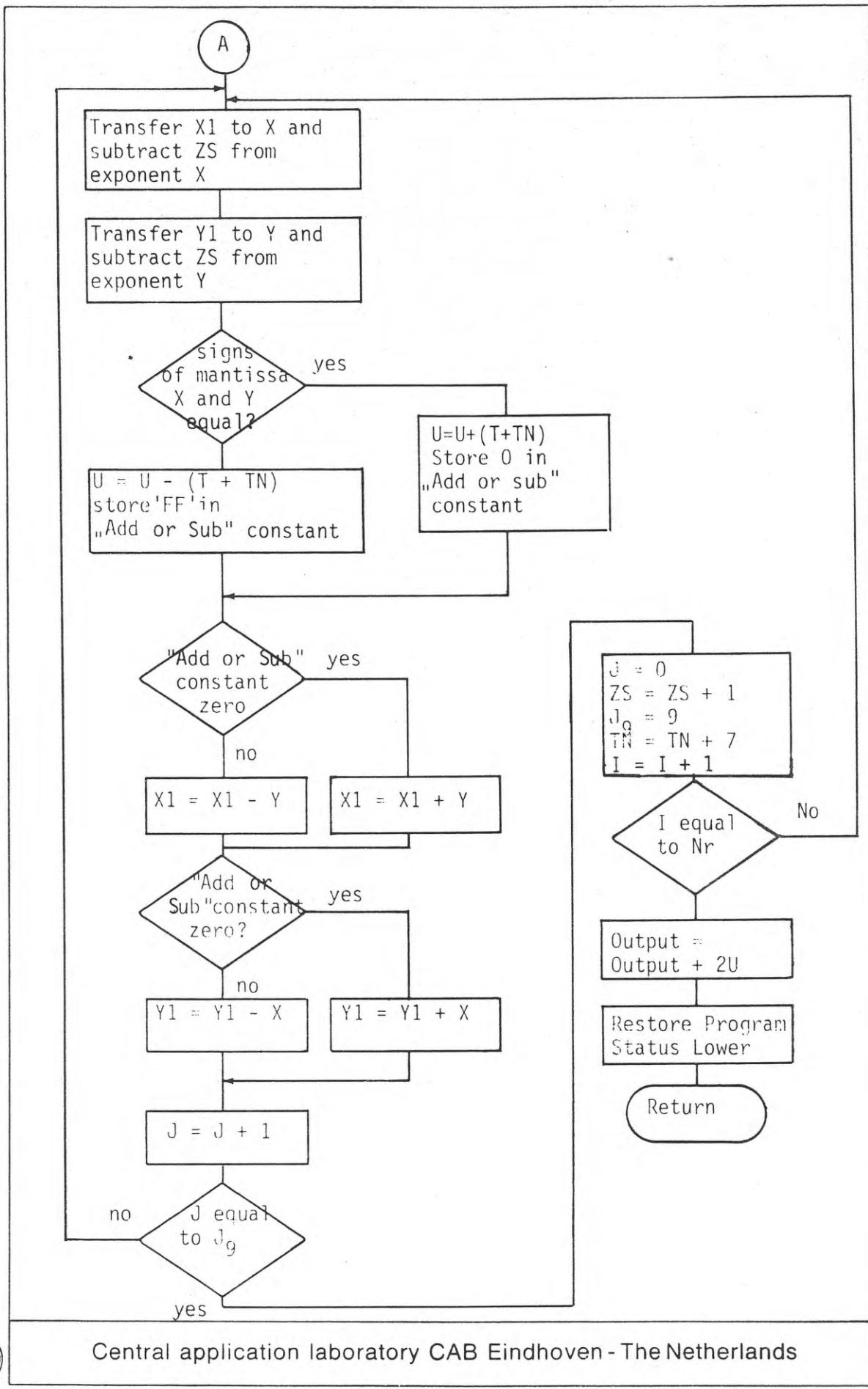
Therefore it is recommended to investigate some other possibilities (other algorithms, binary calculation and conversion to B.C.D. etc.).

.../GS

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## 7. FLOWCHART





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<b>2650 MICROPROCESSOR</b>		<b>ref.no.</b>
<b>Program title</b>	BCD logarithmic routine	
<b>Function</b>	Calculating the $e^{\log}$ of a BCD floating point number $\ln(\text{input operand}) = \text{output result}$	
<b>Parameters:</b>		
<b>    input</b>	The address of byte 0 of the input operand is in R0 and R1. The address of byte 0 of the output results is in R2 and R3.	
<b>    output</b>	Result of $e^{\log}$ in location pointed to by R2, R3.	
<b>Requirements:</b>	None	
<b>    hardware</b>		
<b>    software</b>	Availability of BCD floating point arithmetic package.	
<b>Modified in 2650</b>		
<b>Registers</b>	R0 R1 R2 R3 R1'R2'R3'	<b>Max. Subroutine Nesting Level</b>
	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	1
<b>PSU</b>	F II SP	<b>Assembler</b>
	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<b>PSL</b>	CC IDC RS MC OVF COM C	<b>Memory requirement (bytes)</b>
	<input type="checkbox"/>	<b>RAM</b>
		38
		<b>ROM</b>
		582
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MAIN PROGRAMMER REF. NO. BCD LOGARITHM ROUTINE EDP 7612 PAGE 10/15

LINIE 4000 9870 E SOURCE

```

0524      +
0525      + EDPW 76125-1400
0526      ****+
0527      + BCD LOGARITHMIC ROUTINE +
0528      ****+
0529      +
0530      * THIS ROUTINE CALCULATES THE LOG OF AN INPUT
0531      * NUMBER AND STORES THE RESULT IN AN OUTPUT AREA
0532      +
0533      + CALLING NAME IS 'LOG'
0534      + INPUT ADDRESS MUST BE GIVEN IN R0/R1
0535      * OUTPUT ADDRESS MUST BE GIVEN IN R2/R3
0536      +
0537      * THE ROUTINE USES BCD FLOATING POINT PACKAGE - REPORT EDP7603
0538      * FORMAT OF INPUT AND OUTPUT NUMBER ARE AS REQUIRED
0539      * FOR THIS PACKAGE
0540      +
0541      * IF THE INPUT IS NEGATIVE OR ZERO, A BRANCH IS
0542      + MADE TO LOCATION 'ERR'
0543      +
0544      ****+
0545 0549      000      41000
0546      +
0547 0546      NF      EQU      8      + NUMBER OF OUTER LOOPS
0548      +
0549      + TABLE OF CONSTANTS +
0550      +
0551 0550 000000010      T      DATA      H'00, 00, 00, 10, 00, 25, 55
0552 0004 000525
0553 0553 F0010010      DATA      H'F0, 01, 00, 10, 00, 00, 00
0554 000B 000233
0555 0555 F0020010      DATA      H'F0, 02, 00, 10, 00, 00, 00
0556 0012 000003
0557 0557 00000000      DATA      H'00, 00, 00, 00, 01, 00, 00
0558 0019 010000
0559 0559 00000000      DATA      H'00, 00, 00, 00, 00, 10, 00
0560 0020 001000
0561 0561 00000000      DATA      H'00, 00, 00, 00, 00, 01, 00
0562 0022 00000000      DATA      H'00, 00, 00, 00, 00, 00, 00
0563 0027 000100
0564 0564 00000000      DATA      H'00, 00, 00, 00, 00, 00, 10
0565 002E 000010
0566 0566 00000000      DATA      H'00, 00, 00, 00, 00, 00, 01
0567 0029 000001
0568 0568 00010010      ONE      DATA      H'00, 01, 00, 10, 00, 00, 00
0569 0030 00000000
0570 0570 00000000      II      DATA      H'00, 00, 00, 00, 00, 00, 00
0571 0043 00000000
0572 0572 00010000      LN10      DATA      H'00, 01, 00, 27, 00, 58, 51
0573 0044 025051

```

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THIN ASSEMBLER VER 2.0 EDP LOGARITHM ROUTINE FOR 7412 PAGE 0016

LINE NUMBER OBJECT-E SOURCE

```

0620      * MANTISSA FS +
0624      *
0625 0840  I  RES  1      * INNER LOOP COUNTER
0626 084E  I  RES  1      * NR OF CYCLES (INITIALLY 22)
0627 084F  I  RES  1      * OUTER LOOP COUNTER
0628 0850  TN  RES  1      * NEXT TABLE ITEM
0629 0851  ZS  RES  1      * EXPONENT DECREMENT NR
0630 0852  A09  RES  1      * TEST LOC. REG. IR SUBTR
0631 0853  PSL  RES  1      * STORE LOCATION PSL
0632 0854  Y   RES  7
0633 085B  X1  RES  7
0634 0862  Y   RES  7
0635 0869  Y1  RES  7
0636 0870  OUTP RES  2
0637  *
0638  * SUBROUTINE : DATA POINTERS
0639  * PTR1 FROM R0 R1, PTR2 FROM R2 R3
0640  * PTR3 = PTR1 + 2
0641  *
0642 0871 000440 STFT  STRA R0 PTR1
0643 0875 000441 STRA R1 PTR1+1
0644 0878 0E0442 STRA R2 PTR2
0645 087B 0E0443 STRA R3 PTR2+1
0646 087E 0E0444 STRA R2 PTR2
0647 0881 0002 ADD1 R3 2
0648 0880 0E0445 STRA R2 PTR2+1
0649 0886 17 RETC UN
0650  *
0651  * SUBROUTINE SUBTRACT DS FROM EXPONENT
0652  * R2 CONTAINS SIGN, R3 CONTAINS EXPONENT
0653  * CONDITION CODE ACCORDING TO CONTENTS OF R2
0654  *
0655 0887 1807 SUBE  BCTR Z  EPOS    JUMP IF EXPONENT POSITIVE
0656 0888 0766 ADD1 R2 H'66    IF NEGATIVE ADD DS
0657 0888 0FA051 ADDA R2 ZS          TO EXPONENT
0658 088E 97 CAR1 R3
0659 088F 17 RETC UN
0660 0890 0F0051 EPOS  SUBA R3 ZS    EXPONENT POSITIVE
0661 0893 97 CAR1 R3    SUBTRACT 2 FROM EXPONENT
0662 0894 8501 TPSL  H'01    TEST CARRY
0663 0896 14 RETC R1    IF CARRY RETURN
0664 0897 0766 ADD1 R3 H'66    CALCULATE ORIGINAL EXPONENT
0665 0899 0F0051 ADDA R3 ZS
0666 089C 37 CAR1 R3
0667 089D 0FF0 ADD1 R2 H'FF    CHANGE SIGN OF EXPONENT
0668 089E 0F0051 ADDA R3 ZS    SUBTRACT EXPONENT FROM DS
0669 089F 97 CAR1 R3
0670 08A0 17 SUBT R3
0671 08A4 17 RETC UN

```

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TWIN RECEIVER FOR 2 R EDP LOGARITHMIC ROUTINE EDP 7612 PAGE R 12

L1NE ADD. DATA FOR SOURCE

0670	*	START LOGARITHMIC ROUTINE
0674	*	
0675 0005 000802	D1 06	STRA, R0 Y * STORE INPUT ADDRESS
0676 0008 000802		STRA, R1 Y+1
0677 0008 000870		STRA, R2 OUTP * STORE OUTPUT ADDRESS
0678 000E 000871		STRA, R3 OUTP+1
0679 0001 17		CPSL * SAVE PROGRAM STATUS LOWER
0680 0001 7000850		STRA, R0 PSL
0681 0005 0507		L001, R1 LENG * MOVE INPUT TO X
0682 0007 2000862	MVIN	L00A, R0 X, R1 - AS TEMPORARY STORE
0683 0008 000854		STRA, R0 X, R1
0684 0000 5078		EPNR, R1 MVIN
0685	*	INITIALIZE VARIABLES
0686 00EF 20		0007 R0
0687 0008 000840		STRA, R0 T * T = A
0688 0002 00084F		STRA, R0 I * I = A
0689 0006 000850		STRA, R0 TN * TN = A
0690 0009 0401		L001, R0 I
0691 000B 000851		STRA, R0 DS * DS = 1
0692 000E 0416		L001, R0 Z1
0693 0000 00084E		STRA, R0 Z2
0694 0000 000807		L001, R3 LENG * CLFAR II
0695 0005 20		P007 R0
0696 0004 00487F	D1 R1	STRA, R0 X, R1 -
0697 0009 5078		EPNR, R2 D1 R1
0698	*	
0699 0008 0507		L001, R1 LENG * CLFAR OUTPUT
0700 0000 20		P007 R0
0701 000E 000870	CLFD	STRA, R0 XOUTP, R1 -
0702 0001 5078		EPNR, R1 CLFD
0703	*	
0704	*	DECREESE EXPONENT TILL 00
0705	*	ADD 1 IF EXP POSITIVE OR
0706	*	SUBTRACT 1 IF EXP NEGATIVE
0707	*	LN10 TO DR FROM OUTP
0708	*	
0709 0003 7508	DECE	CPSL WC * WITHOUT CARRY
0710 0005 0501		L001, R1 I * LOAD INDEX FOR EXPONENT
0711 0007 000854		L00A, R0 X, R1 * LOAD EXPONENT
0712 000A 1308		P0TR, I CONT * IF ZERO CONTINUE
0713 000C 0401		SUB1, R0 I * SUBTRACT 1 FROM EXPONENT
0714 00EF 24		DR, R0 * DECIMAL ADJUST
0715 00EF 000854		STRA, R0 X, R1 * STORE DECREASED EXPONENT
0716 00F2 000870		L00A, R0 OUTP * LOAD POINTERS FOR
0717 00F5 000871		L00A, R1 OUTP+1 ADDING OR SUBTRACTING
0718 00F8 000446		STRA, R0 PTER * LN10 TO DR FROM OUTP
0719 00FF 000447		STRA, R1 PTER+1
0720 00FF 0000		L001, R2 LN10
0721 0000 0000		L001, R3 LN10
0722 0000 000870		P0TR, I N STFT

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TWIN ASSEMBLER VER 2.0. (C) - MARCH 1970 ROUTINE (EDP 7612) - PAGE 0018

## LINE ADDR OBJECT F SOURCE

0724 0905 0C0854	LODA, R0 X	* LOAD SIGN EXPONENT	
0725 0908 1805	BCTR, Z LADD	* IF POSITIVE ADD	
0726 0909 3F0469	BSTA, UN DEIR		
0727 0900 1854	BCTR, UN DECE		
0728 090F 3F0470	LADD	BSTA, UN DRDD	
0729 0912 1B4F	BCTR, UN DECE		
0730 0914 20	CONT	EDRZ RA	* MAKE SIGN OF EXPONENT POSITIVE
0731 0915 0C0854		STRA, R0 X	
0732	*		
0733	*	TEST MANTISSA FOR NEGATIVE, ZERO OR ONE	
0734	*	IF NEGATIVE OR ZERO, JUMP TO FPR	
0735	*	IF MANTISSA IS ONE / NORMALIZED INPUT	
0736	*	THEN IS A 11, SUBTRACT LN10 FROM OUTPUT	
0737	*	AND RETURN	
0738	*		
0739 0918 0C0856	LODA, R0 X+2	* TEST SIGN MANTISSA	
0740 0918 0C087CB	BCFA, Z FPR	* IF NEG, JUMP TO FPR	
0741 091E 0507	LODI, R1 LPNG		
0742 0900 004854	TSTZ	LODA, R0 X, R1,-	* LOAD DIGIT OF MANTISSA
0743 0920 0C085E	BCFA, Z TST0	* IF NOT ZERO, TEST FOR 1	
0744 0920 E503	COMI, R1 1	* END OF MANTISSA?	
0745 0920 0C08920	BCFA, E0 TSTZ	* IF NOT, KEEP TESTING	
0746 0920 1F07CB	BSTA, UN FPR	* JUMP TO FPR	
0747 0920 E503	TST0	COMI, R1 1	* FIRST BYTE OF MANTISSA?
0748 0920 0C08952	BCFA, E0 CTN	* IF NOT, CONTINUE	
0749 0913 E410	COMI, R0 H 101	* ONE?	
0750 0925 0C08953	BCFA, E0 CTN	* IF NOT, CONTINUE	
0751 0928 0C08870	LODA, R0 OUTP	* LOAD POINTERS	
0752 0928 0D0871	LODA, R1 OUTP+1		
0753 093E 0C08446	STRA, R0 PTRR		
0754 0941 CD0447	STRA, R1 PTRR+1		
0755 0944 0608	LODI, R2 LN10		
0756 0946 0746	LODI, R2 LN10		
0757 0948 3F0872	BSTA, UN STPT		
0758 0948 3F0469	BSTA, UN DSUB	* OUTPUT - LN10	
0759 094E 0C08653	LODA, R0 PSL	* RESTORE PROGRAM STATUS	
0760 0951 93	LPSL		
0761 0952 17	RETO, UN	* RETURN	
0762 0952 0408	CTN	LODI, R0 CX	* LOAD POINTER NORMALIZED
0763 0955 0554		LODI, R1 CX	INPUT
0764 0957 0608		LODI, R2 CXNE	* LOAD POINTER CONSTANT 1
0765 0959 0738		LODI, R2 CXNE	
0766 095B 3F0872	BSTA, UN STPT		
0767 095E 0408	LODI, R0 CX1	* LOAD POINTER 'X1'	
0768 0960 0558	LODI, R1 CX1		
0769 1962 0C08446	STRA, R0 PTRR		
0770 0965 0C08447	STRA, R1 PTRR+1		
0771 0963 3F0469	BSTA, UN DSUB	* X1 = INPUT - 1	

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TWIN ASSEMBLER VER 2.0 RCD LOGARITHM ROUTINE (EDP 7612) PAGE 0019

LINE ADDR OBJECT E SOURCE

```

0773 096B 0408 LODI.R0 X1      * LOAD POINTER Y1
0774 096D 0569 LODI.R1 X1
0775 096F C00446 STRA.R0 PTRR
0776 0972 C00447 STRA.R1 PTRR+1
0777 0975 3F0470 BSTA.UN DADD      * Y1 = INPUT + 1
0778 *
0779 * X = X1 * 10^(EXP-ZS)
0780 *
0781 0978 7508 LOOP OPSL NC      * WITHOUT CARRY
0782 0978 070F LODI.R2 LENG-1    * MOVE Y1 TO X
0783 097C 0FF858 MOVX LODA.R0 X1,R3
0784 097F 0F6854 STRA.R0 X,R3
0785 0982 FB78 BOPR.R3 MOVX
0786 0984 0F0850 LODA.R2 X1+1    * EXPONENT
0787 0987 0E0858 LODA.R2 Y1      * SIGN OF EXPONENT
0788 098A 3F0887 BSTA.UN SUBE    * DECREMENT EXPONENT X
0789 098D C00854 STRA.R2 X      * STORE SIGN
0790 0990 0F0855 STRA.R3 X+1    * STORE EXPONENT
0791 *
0792 * Y = Y1 * 10^(EXP-ZS)
0793 *
0794 0993 0706 LODI.R3 LENG-1    * MOVE Y1 TO Y
0795 0995 0F6869 MOVY LODA.R0 Y1,R3
0796 0998 0F6862 STRA.R0 Y,R3
0797 099B FB78 BOPR.R3 MOVY
0798 099D 0F0868 LODA.R3 Y1+1    * EXPONENT
0799 09A0 0E0869 LODA.R2 Y1      * SIGN OF EXPONENT
0800 09A3 3F0887 BSTA.UN SURE    * DECREMENT EXPONENT Y
0801 09A6 C00862 STRA.R2 Y      * STORE SIGN
0802 09A9 0F0863 STRA.R3 Y+1    * STORE EXPONENT
0803 *
0804 * U = U +/- T(I)
0805 *
0806 09AC 0408 LODI.R0 CU      * LOAD POINTERS
0807 09AE 053F LODI.R1 CU
0808 09B0 C00446 STRA.R0 PTRR
0809 09B3 C00447 STRA.R1 PTRR+1
0810 09B6 0608 LODI.R2 CT      * NEXT CONSTANT FROM TABLE
0811 09B8 0F0850 LODA.R3 TN
0812 09B8 8700 ADDI.R3 DT
0813 09BD 3F0872 BSTA.UN STPT
0814 * DETERMINE ADDITION OR SUBTRACTION
0815 09CB 0C0856 LODA.R0 X+2    * COMPARE SIGNS OF MANTISSAE
0816 09C3 EC0864 COMA.R0 Y+2
0817 09C6 9806 BCPR.EQ SUBM    * IF NOT EQUAL, JUMP TO SUBM
0818 09C8 3F0470 BSTA.UN DADD    * OTHERWISE ADD
0819 09CB 20 EORZ R0
0820 09CC 1805 BCTR.UN CTN1    * CONTINUE
0821 09CE 3F0469 SUBM BSTA.UN DSUB
0822 09D1 04FF LODI.R0 H FF
0822 09D3 C00852 CTN1 STRA.R0 ADS      * STORE BRANCH CONSTANT

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TWIN ASSEMBLER VER 2.0 BCN LOGARITHM ROUTINE (EDP 7612) PAGE NO.20

LINIE ADDR. OBJECT E SOURCE

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0825      * X1 = X1 +/- Y
0826      *
0827 0906 0408 LODI,R0 CX1      * LOAD POINTERS
0828 0908 0558 LODI,R1 CY1
0829 0909 C00446 STRA,R0 PTRR
0830 0900 C00447 STRA,R1 PTRR+1
0831 09E0 0608 LODI,R2 CY
0832 09E2 0762 LODI,R3 CY
0833 09E4 3F0872 BSTA,UN STPT
0834      * DETERMINE ADDITION OR SUBTRACTION
0835 09E7 0C00852 LODA,R0 A0S      * LOAD BRANCH CONSTANT
0836 09E8 0805 BCFR,Z ADDM      * IF NOT ZERO, JUMP TO ADDM
0837 09E0 3F0469 BSTA,UN DSUB
0838 09EF 1B03 BCTR,UN CTN2      * CONTINUE
0839 09F1 3F0470 ADDM BSTA,UN DADD
0840      *
0841      * Y1 = Y1 +/- X
0842      *
0843 09F4 0408 CTN2 LODI,R0 CY1      * LOAD POINTERS
0844 09F6 0569 LODI,R1 CY1
0845 09F8 C00446 STRA,R0 PTRR
0846 09FB C00447 STRA,R1 PTRR+1
0847 09FE 0608 LODI,R2 CX
0848 09AA 0754 LODI,R3 CY
0849 09A2 3F0872 BSTA,UN STPT
0850      * DETERMINE ADDITION OR SUBTRACTION
0851 0A05 0C00852 LODA,R0 A0S      * LOAD BRANCH CONETANT
0852 0A08 3805 BCFR,Z ADDN      * IF NOT ZERO, JUMP TO ADDN
0853 0A0A 3F0469 BSTA,UN DSUB
0854 0A0D 1B03 BCTR,UN CTNS      * CONTINUE
0855 0A0F 3F0470 ADDN BSTA,UN DADD
0856      *
0857      * COMMON PART
0858      *
0859 0A12 7508 CTNE CPSL NC      * WITHOUT CARRY
0860 0A14 0C0084D LODA,R0 J      * J = I + 1
0861 0A17 3401 ADDI,R0 1
0862 0A19 C00084D STRA,R0 T
0863 0A1C E00084E COMA,R0 T9      * COMPARE WITH T9
0864 0A1F 900978 BCFA,EQ LOOP      * IF LESS LOOP
0865 0A22 29 EORZ R0      * RESTORE J TO R
0866 0A23 C00084D STRA,R0 T
0867 0A26 0C00851 LODA,R0 ZS      * ADD 1 TO ZS
0868 0A29 3401 ADDI,R0 1
0869 0A2B 0C00851 STRA,R0 ZS
0870 0A2E 0409 LODI,R0 9      * J9 = 9
0871 0A30 C00084E STRA,R0 T9
0872 0A32 0C00850 LODA,R0 TN      * ADD 7 TO TN FOR NEXT CONSTANT
0873 0A36 3407 ADDI,R0 7
0874 0A38 C000850 STRA,EQ TN

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TWIN ASSEMBLER VER 2.0 BCD LOGARITHM ROUTINE (EDP 7612) PAGE 0021

LINE ADDR OBJECT E SOURCE

0876 0A2B 0C084F	L0DA, R0 I	* ADD 1 TO I
0877 0A2E 0A01	ADDI, R0 1	
0878 0A40 0C084F	STRA, R0 I	
0879 0A43 E408	COMI, R0 NR	* COMPARE WITH NR
0880 0A45 0C0873	BCFA, E0 LOOP	* IF LESS THEN LOOP
0881 *		
0882 *		
0883 *	DUTP = DUTP + 2U	
0884 *		
0885 0A48 0C0870	L0DA, R0 DUTP	* LOAD POINTERS
0886 0A4B 0D0871	L0DA, R1 DUTP+1	FOR ADDING U TWO
0887 0A4E 0C08446	STRA, R0 PTRR	TIMES TO DUTP
0888 0A51 0C08447	STRA, R1 PTRR+1	
0889 0A54 A608	L0D1, R2 <II	
0890 0A56 073F	L0D1, R3 >I	
0891 0A58 3F0872	RSTA, UN STPT	
0892 0A58 3F0470	RSTA, UN DADD	* ADD
0893 0A5E 3F0470	RSTA, UN DADD	* ADD
0894 0A61 0C08853	L0DA, R0 PSL	* RESTORE PROGRAM STATUS
0895 0A64 93	LPSL	
0896 0A65 17	RETC, UN	* RETURN
0897 *		
0898 0A00	END A	

TOTAL ASSEMBLY ERRORS = 0000

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